IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SYNOPSYS, INC., a Delaware Corporation, Plaintiff and Counter-Defendant, v. MAGMA DESIGN AUTOMATION, INC., a Delaware Corporation Defendant and Counterclaimant.	C.A. No. 05-701 GMS

DECLARATION OF WILLIAM J. WADE

William J. Wade declares as follows:

1. I am a director in the law firm of Richards Layton & Finger, P.A., Delaware counsel to defendant and counterclaim plaintiff Magma Design Automation, Inc. in this action.

2. Attached hereto as Exhibit A is a true and correct copy of a report entitled *Synopsys Files Two Additional Suits Against Magma* as published on the Programmable Logic Design Line website on September 27, 2005.

3. Attached hereto as Exhibit B is a report entitled *Synopsys Strikes at Magma's Cobra* as published on the Electronic News website on September 28, 2005.

4. Attached hereto as Exhibit C is a true and correct copy of the March 24, 2001 PTO Office Action Summary by which the Examiner rejected all pending claims of the '355 application.

5. Attached hereto as Exhibit D is a true and correct copy of the introductory pages of the proceedings of the 14th IEEE VLSI Test Symposium held on April 28 through May 1, 1996 in Princeton, New Jersey.

6. Attached hereto as Exhibit E is a true and correct copy of the introductory pages of the Proceedings of the IEEE European Test Workshop held at Montpellier, France on July 12-14, 1996.

7. Attached hereto as Exhibit F is a true and correct copy of Ex Parte Reexamination Filing Data – March 31, 2005 as published by the Commissioner for Patents, United States Patent and Trademark Office.

I declare under penalty of perjury that the foregoing is true and correct.

William J. Wade

Dated: February 6, 2006

EXHIBIT A

CMP
PROGRAMMABLE LOGIC DesignLine

September 27, 2005

Synopsys files two additional suits against Magma

By Dylan McGrath
SAN FRANCISCO — Synopsys Inc. has filed two additional lawsuits in its high-profile patent dispute with rival Magma Design Automation Inc.

Synopsys (Mountain View, Calif.) Monday (Sept. 26) filed a claim of unfair competition against Magma in California Superior Court in Santa Clara County as well as a complaint in U.S. District Court for the District of Delaware claiming that Magma infringes three patents held by Synopsys.

Yvette Huygen, Synopsys' worldwide public relations manager, said Wednesday that the company filed the Delaware suit because, during the discovery process of the ongoing trial, Synopsys came to believe that Magma's alleged IP infringement went further than Synopsys initially thought. The Santa Clara lawsuit, Huygen said, was filed in the name of preserving fair business practices because Synopsys believes that Magma has made conflicting public statements.

"This whole thing has been, and continues to be, about protecting intellectual property," Huygen said.

David Stanley, Magma's special counsel, said that Magma does not practice any of the methodologies contained in the three patents named in the Delaware suit. He added that the company has found extensive prior art usage of two of the patents and is continuing research on the third. Prior art usage, if proven, could invalidate the claim of patent infringement.

Stanley said the unfair business practice suit is similar to claims Synopsys has already filed against Magma in U.S. District Court. He said he believes Synopsys filed this suit in state court because it did not think it could win the case currently being argued in U.S. District Court.

Both Stanley and Roy Jewell, Magma president and chief operating officer, characterized the latest Synopsys actions as "desperate" tactics.

"We see it as an example of [Synopsys'] continuing abuse of the legal system to try to gain a competitive advantage in an unfair way," Stanley said.

Synopsys and Magma (Santa Clara, Calif.) have been involved in a contentious, often bitter patent dispute since September 2004. Synopsys claims that technology that was originally developed at Synopsys underlies Magma products, which Magma disputes.

In the saga's most recent chapter, a U.S. District Court in August issued a restraining order preventing Magma from abandoning or seeking re-examination of the two patents at the heart of the litigation.

EXHIBIT B

Reed Electronics Group

ElectronicNews
Your World in Real Time
February 1, 2006

Synopsys Strikes at Magma's Cobra

Related Articles
- Court Deals Magma a Blow in Synopsys Litigation
- Magma Claims Patents in Synopsys Dispute Jointly Owned by IBM
- Magma Accuses Synopsys of Antitrust Violations
- Commerce Dept Unveils Plan to Counter IP-Theft

TOP HEADLINES
- Valley's Lobbying Pays Dividends
- Will Dell Deal with AMD?
- NEC Teams with Sony. Toshiba on 45nm
- Tower Staggered by $200M Loss
- ST Targets Sales, Market Share
- PortalPlayer Looks to India
- NTT DoCoMo Develops Prototype HSDPA Handsets
- Special Charges Drag on Flextronics Profits

By Ann Steffora Mutschler -- *Electronic News*, 9/28/2005

Buried among a number of product announcements it made Monday, Synopsys Inc. quietly filed two more lawsuits including another patent infringement suit against rival Magma Design Automation.

The patent infringement suit was filed in Delaware, where both companies are incorporated, concerns three patents, the first of which is U.S. patent number 6,192,508, that Synopsys gained with its 2004 acquisition of Monterey Design Systems. The second patent is U.S. patent number 6,434,733 that was issued to the company in August 2002. The third patent is U.S. patent number 6,766,501, which was issued to Synopsys in July 2004.

Article continues below

According to the filing, Synopsys believes Magma has been and still is infringing the patents in its Cobra and Blast Fusion products.

Synopsys spokeswoman Yvette Huygen said the suit has always been about protecting Synopsys' IP. "During the discovery process in the existing suit, we discovered Magma's patent infringement went further than we thought," she said in regard to this additional filing.

The second suit was filed by Synopsys in Santa Clara County Superior Court in California alleging unfair competition, based on Magma's actions in defending itself in the federal patent case between the companies.

Tuesday, Magma issued a statement saying that it believes these suits are "without merit and

Highlights
Reed Electronics Group Research
Site Membership
Welcome, Guest
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Newsletters
Free Newsletters
Resources
Archives
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indicative of 'desperate' tactics by Synopsys.

"These actions are questionable, perhaps laughable, and indicative of an increasingly desperate strategy by Synopsys to maintain market share," said Magma president and COO Roy Jewell, in a statement.

"They likely concluded that their current case is weak -- because of validity and ownership issues, to name just two -- and so are attempting to bolster it by piling on these dubious claims. We're truly disappointed to see these latest actions by Synopsys, given that the industry already suffers from a reputation for excessive litigation," he continued.

Jewell also said he was, "troubled that a company that was once the leader in our industry has resorted to these egregious tactics to defend a declining market position against an up-and-coming innovator like Magma."

Magma's special counsel David Stanley noted that bringing an action on the basis of the Monterey patent (the '508 patent) is especially strange since Synopsys was asked specifically at the time it acquired Monterey last year if it would use the Monterey patents in its litigation against Magma. Synopsys apparently said they would not, Stanley said.

"But even more incredible -- if that is possible -- is the claim of unfair competition in the California filing," Stanley added. "If one is to believe Synopsys, it is 'unfair' for anybody to mount a defense when sued."

"I can only hope this strategy is the result of a legal team out of control. I think it is time to challenge the EDA industry leaders to abandon their litigious tendencies as a competitive strategy and refocus on what is truly important: customer success. Only in this way can we continue building value for our customers, shareholders and employees," Jewell concluded.

Synopsys countered by noting that the second suit was filed to preserve fair business practices. "Magma has been making contradictory public statements, which has created an unfair business environment," Huygen concluded.

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EXHIBIT C

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/283,795	03/31/99	MUGGIRALA	SNSY-A1998-0

TM02/0419

WAGNER, MURABITO & HAO
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
REDSON, H	
ART UNIT	PAPER NUMBER
2153	4

DATE MAILED: 04/19/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

PTO-90C (Rev. 11/00) 1 File Copy

Office Action Summary	Application No 09/283,095	Applicant(s) Duggirala et al.
	Examiner Walter Benson	Art Unit 2153

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.

2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-22 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1 ☐ Certified copies of the priority documents have been received.

2 ☐ Certified copies of the priority documents have been received in Application No. _____.

3 ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

1. Claims 1-22 are presented for examination

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3 Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack proper antecedent basis:

i. --coupled said first functional pin– c), claim 1

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

5 Claims 1, 9, 13, 18, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Narayanan et al. (US Patent No. 5,983,376 and hereinafter Narayanan)

6. As Claims 1, 9, 13, 18, and 19, Narayanan discloses an electronic design automation system [Fig. 3] and computer implemented method of constructing a scan chain, said method comprising:

a) receiving a netlist description of an integrated circuit design having a plurality of functional pins (col. 2, lines 29-39 and col 5, lines 31-33) ;

b) inserting scan cells to said netlist description, said scan cells being coupled serially together to form a scan chain (col. 2, lines 32-34);

c) placing said scan cells to determine a cell layout, wherein said step (c) is performed without regard to any predetermined constraint designating a functional pin as a scan-in port and without regard to any

predetermined constraint designating a functional pin as a scan-out port of said scan chain (col. 1, lines 61-66; col. 4, lines 62-67 and col 5, lines 1-3);

d) based on said cell layout of said step (c), selecting a first functional pin of said plurality of functional pins to be a scan-in port of said scan chain (col. 11, lines 15-17);

e) modifying said netlist description to coupled said first functional pin to a leading scan cell of said scan chain (col. 11, lines 17-21)

Claim Rejections - 35 USC § 103

7 The following is a quotation of 35 U.S C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made

8 Claims 2-8, 10-12, 14-17, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narayanan et al. (US Patent No 5,983,376 and hereinafter Narayanan) as applied to claims 1,9,13,18, and 19 above, and further in view of Giles et al. (US Patent No. 5,812,561 and hereinafter Giles)

9. As to claims 2, 10, and 20, the system disclosed by Narayanan shows substantial features of the claimed invention (discussed above) although it fails to disclose:

wherein said first functional pin is selected according to a position of said, leading scan cell of said scan chain relative to said plurality of functional pins.

Nonetheless, these features are well known in the art and would have been an obvious modification of the system disclosed by Narayanan, as evidenced by Giles.

In an analogous art Giles discloses a computer implemented system of constructing a scan chain, wherein said first functional pin is selected according to a position of said, leading scan cell of said scan chain relative to said plurality of functional pins (Fig. 2; col. 6, lines 47-49).

Given the teaching of Giles, a person having ordinary skill in the art would have readily recognized the desirability and advantages of modifying Narayanan by employing the well known conventional features of scan techniques, such as disclosed by Giles to efficiently provide an improved testable design for an Integrated Circuit device.

10. As to claims 3, 11, and 21, Giles discloses a system wherein said step (d) further comprises:

d1) determining a functional pin of said plurality of functional pins that is closest to said leading scan cell (col. 6, lines 49-51);

d2) selecting said first functional pin to be said functional pin determined at step (d1) (col. 6, lines 65-67).

11 As to claims 4, 12, and 22, Giles discloses a system wherein said step (e) further comprises:

e1) inserting a multiplexer within said netlist description (col 7, lines 1-6);

e2) coupling said first functional pin to said leading scan cell via said multiplexer (217, Fig.2).

12. As to claims 5 and 14, Giles discloses a system further comprising:

f) based on said cell layout of said-step (c), selecting a second functional pin of said plurality of functional pins to be a scan-out port of said scan chain (col. 7, lines 10-17);

g) modifying said netlist description to couple said second functional pin to a last scan cell of said scan chain (col 7, lines 29-35).

13. As to claims 6 and 15, Giles discloses a system wherein said second functional pin is selected according to a position of said last scan cell of said scan chain relative to said plurality of functional pins (211, Fig 3; col 7, lines 35-38)

14 As to claims 7 and 16, Giles discloses a system wherein said step (f) further comprises:

f1) determining a functional pin of said plurality of functional pins that is closest to said last scan cell (col 6, lines 50-51);

f2) selecting said second functional pin to be said functional pin determined at step (f1) (col. 7, lines 19-22).

15. As to claims 8 and 17, Giles discloses a system wherein said step (e) further comprises:

e1) inserting a multiplexer within said netlist description (Fig. 2; col. 7, lines 45-50);

e2) coupling said second functional pin to said last scan cell via said multiplexer (Col 7, lines 59-62).

Prior Art Made of Record

A. Chakradhar et al (US Patent No. 5,726,996) discloses methods, software, and apparatus for dynamic composition and test cycle reduction;

B. Beausang et al. (US Patent No. 6,067,650) discloses a method and apparatus for performing partial unscan and near full scan within design for test applications.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter Benson whose telephone number is (703) 306-4525 The examiner can normally be reached on Monday to Thursday and alternate Fridays from 6:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith, can be reached on (703) 308-1323 The fax phone number for the organization where this application or proceeding is assigned is (703) 305-7201.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-3900.

Walter Benson WB
Patent Examiner
April 12, 2001

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Notice of References Cited	Applicant/Patent: Duggirala et al.	Application/Control No: 09/283,095	
	Examiner: Walter Benson	Art Unit: 2153	Page 1 of 1

U.S. PATENT DOCUMENTS

		Document Number Country Code-Number-Kind Code	Date MM-YYYY[1]	Name	Classification[2]	
	A	5,983,376	11/1999	Narayanan et al.	714	726
	B	5,812,561	9/1998	Giles et al.	714	726
	C	5,726,996	3/1998	Chakradhar et al.	714	724
	D	6,067,650	5/2000	Beausang et al.	714	726
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

		Document Number Country Code-Number-Kind Code	Date MM-YYYY[1]	Country	Name	Classification[2]	
	N						
	O						
	P						
	Q						
	R						
	S						
	T						

NON PATENT DOCUMENTS

		Include, as applicable: Author, Title, Date, Publisher, Edition or Volume, Pertinent Pages
	U	"A New Approach to Scan Chain Reordering Using Physical Design Information." Beausang et al. . International Test Conference. IEEE. 1998
	V	"Scan Insertion Criteria for Low Design Impact" Barbagallo et al ,14th VLSI Test Symposium. IEEE. 1996.
	W	
	X	

* A copy of this reference is not being furnished with this Office action. See MPEP § 707.05(a). [1] Dates in MM-YYYY format are publication dates. [2] Classifications may be U.S. or foreign.

Form PTO-948 (REV 10-97) U.S. DEPARTMENT OF COMMERCE-Patent and Trademark Office Application No 293095

NOTICE OF DRAFTPERSON'S PATENT DRAWING REVIEW

The drawing filed (insert date) 3/3/97 are:

a. ___ not objected to by the Draftperson under 37 CFR 1.84 or 1.152.

b. X objected to by the Draftperson under 37 CFR 1.84 or 1.152 as indicated below. The Examiner will require submission of new, corrected drawings when necessary. Corrected drawings must be submitted according to the instructions on the back of this notice.

1. DRAWINGS. 37 CFR 1.84(a): Acceptable categories of drawings:
Black ink. Color.
Color drawings are not acceptable until petition is granted.
Fig(s) ___
Pencil and non-black ink not permitted. Fig(s) ___
2. PHOTOGRAPHS. 37 CFR 1.84(b)
Photographs are not acceptable until petition is granted.
Glossy finish not acceptable. Fig(s) ___
Heavy, glossy, white paper, mounted photographs or photographs with dark backgrounds not acceptable. Fig(s) ___
Poor quality (half-tone). Fig(s) ___
3. SIZE OF PAPER. 37 CFR 1.84(f)
Paper not flat, pliable, strong, white, and durable.
Fig(s) ___
Erasures, alterations, overwriting, interlineations, folds, copy machine marks not acceptable. (too thin)
Mylar material not acceptable. (too thin)
Fig(s) ___
4. SIZE OF PAPER. 37 CFR 1.84(f). Acceptable sizes:
21.0 cm by 29.7 cm (DIN size A4)
Letter size (8 1/2 x 11 inches)
All drawings sheets not the same size.
Sheet(s) ___
5. MARGINS. 37 CFR 1.84(g): Acceptable margins:
Top 2.5 cm (1 inch) Right 1.5 cm Bottom 1.0 cm
SIDE EDGE SIZE
Top 2.5 cm (1 inch) Right 1.5 cm Bottom 1.0 cm
MAXIMUM SIZE
Margins not acceptable. Fig(s) ___
Top (T) ___ Left (L) ___
Right (R) ___ Bottom (B) ___
6. VIEWS. 37 CFR 1.84(h)
REMINDER: Specification may require revision to correspond to drawing changes.
Views connected by projection lines or lead lines. Fig(s) ___
7. ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
Brackets needed to show figure as one entry. Fig(s) ___
Views not labeled properly or properly. Fig(s) ___
Enlarged view not labeled properly or properly. Fig(s) ___

7 SECTIONAL VIEWS. 37 CFR 1.84(h)(3)
___ Hatching not indicated for sectional portions of an object. Fig.(s) ___
___ Sectional designation should be noted with Arabic or Roman numbers. Fig.(s) ___
8 ARRANGEMENT OF VIEWS. 37 CFR 1.84(i)
___ Words do not appear on a horizontal, left-to-right fashion when page is either upright or turned so that the top becomes the right side, except for graphs. Fig.(s) ___
___ Views not on the same plane on drawing sheet. Fig.(s) ___
9 SCALE. 37 CFR 1.84(k)
___ Scale not large enough to show mechanism without crowding when drawing is reduced in size to two-thirds in reproduction. Fig.(s) ___
10 CHARACTER OF LINES, NUMBERS, & LETTERS. 37 CFR 1.84(l)
X Lines, numbers & letters not uniformly thick and well defined, clean, durable and black (poor line quality). Fig(s) 4/4 – 8/8
11 SHADING. 37 CFR 1.84(m)
___ Solid black areas pale. Fig.(s) ___
___ Solid black shading not permitted. Fig.(s) ___
___ Shade lines, pale, rough and blurred. Fig.(s) ___
12 NUMBERS, LETTERS, & REFERENCE CHARACTERS. 37 CFR 1.48(p)
___ Numbers and reference characters not plain and legible. Fig.(s) ___
___ Figure legends are poor. Fig.(s) ___
___ Numbers and reference characters not oriented in the same direction as the view. 37 CFR 1.84(p)(3) Fig.(s) ___
___ English alphabet not used. 37 CFR 1.84(p)(3) Fig.(s) ___
X Numbers, letters and reference characters must be at least 32 cm (1/8 inch) in height. 37 CFR 1.84(p)(3) Fig.(s) ___
13 LEAD LINES. 37 CFR 1.84(q)
___ Lead lines cross each other. Fig.(s) ___
___ Lead lines missing. Fig.(s) ___
14 NUMBERING OF SHEETS OF DRAWINGS. 37 CFR 1.84(t)
___ Sheets not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig.(s) ___
15 NUMBERING OF VIEWS. 37 CFR 1.84(u)
___ Views not numbered consecutively, and in Arabic numerals, beginning with number 1. Fig.(s) ___
16. CORRECTIONS. 37 CFR 1.84(w)
___ Corrections not made from PTO 948 dated ___
17 DESIGN DRAWINGS. 37 CFR 1.152
___ Surface shading shown not appropriate. Fig.(s) ___
___ Solid black shading not used for color contrast. Fig.(s) ___

COMMENTS:

REVIEWER ___ DATE 7/10/99 TELEPHONE NO 703-305-8995

ATTACHMENT TO PAPER NO 4

PTO COPY

EXHIBIT D

14th IEEE

VLSI TEST SYMPOSIUM

April 28–May 1, 1996
Princeton, New Jersey

Sponsored by
IEEE Computer Society Technical Committee on Test Technology
IEEE Philadelphia Section

IEEE COMPUTER SOCIETY 50 YEARS OF SERVICE 1946-1996

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

Proceedings

14th IEEE
VLSI Test Symposium

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14th IEEE
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April 28 – May 1, 1996

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IEEE Computer Society
13, Avenue de l'Aquilon
B-1200 Brussels
BELGIUM
Tel:, +32-2-770-2198
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IEEE Computer Society
Ooshima Building
2-19-1 Minami-Aoyama
Minato-ku, Tokyo 107
JAPAN
Tel:, +81-3-3408-3118
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The Institute of Electrical and Electronics Engineers, Inc.

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Coordinator: D. Nikolos, University of Patras

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Coordinator: A. Majumdar, Sunrise Test Systems

Panel Session 1:

Moderator: *E. McCluskey, Stanford University*

Coordinators: *J.P. Hayes, Univ. of Michigan and R. Chandramouli, LogicVision*

Panelists: *R. Aitken, Hewlett-Packard*
J. Hutcheson, VLSI Research, Inc.
N. Murthy, Chromatic
P. Nigh, IBM
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Session 9: Delay Fault Testing

Moderator: M.R. Mercer, Texas A&M University

Coordinator: D. Bhattacharya, Texas Instruments

Session 10: Non-Traditional Testing

Moderator: K. Wagner, Synopsys

Coordinator: C. Mallipeddi, Cadence

Panel Session 3:

Co-Organized with Design&Test of Computers

Moderator: *Y. Savaria, Ecole Polytechnique de Montréal*

Coordinator: *A. Ivanov, University of British Columbia*

Panelists: *R.L. Campbell, AT&T Bell Laboratories*
P. Kuekes, Hewlett-Packard
D. Lepejian, HPL
W. Maly, Carnegie Mellon University
M. Nicolaidis, TIMA
A. Orailoglu, University of California, San Diego

Foreword

Welcome to the 1996 IEEE VLSI Test Symposium, the fourteenth in a series that explores exciting new state-of-the-art test concepts, methodologies, and trends in testing electronic circuits and systems. The competitive drive to integrate a wide range of capabilities into compact electronic products as well as the continuous drive to ensure high-quality products has caused the use of traditional means to test electronic products and meet their quality requirements to be much more difficult.

The theme of this year's symposium is "Test Technology for Built-In Quality," and the focus is on novel approaches for integrating designs with built-in capabilities to test and provide quality detection information. The technology to provide integration of a wide range of functions into compact electronic products will be addressed by our renowned keynote speaker, Joseph Borel, Executive Vice President, Central R/D SGS-Thomson, who will discuss the issues involved in designing and manufacturing complex systems on silicon. In order to further enrich the program with information dealing with future trends in microelectronics, VTS has — for the first time — included an invited talk in its technical program. Therefore, technological challenges to create complex systems in the future will be addressed by our invited speaker, Kamran Eshraghian, Foundation Professor at Edith Cowan University and The University of Adelaide, South Australia.

The organizers have arranged a three-day program with two paper presentation sessions running concurrently. These sessions cover hot topics such as Synthesis for Testability, On-Line Testing, BIST, MCM Testing, Mixed-Signal Test, Fault Diagnosis, and IDDQ Testing. In addition, as panel sessions have proven to be very popular with VTS participants, this year we decided to increase the number of panel sessions from six to eight. We are proud to announce that these panels are comprised of expert practitioners from both industry and academia who will discuss relevant issues affecting the field of VLSI test technology both now and in the future. In conjunction with TTTC, two tutorials on design verification and new trends in design are also being offered. These timely topics were selected from a long list of proposed subjects based on their high level of interest to many in our audience.

With the increasing flow of top-quality submissions, paper selection continues to be a difficult task. The papers for VTS'96 were selected on the basis of a rigorous review procedure with more than 325 reviewers participating in the process. The final selection was made by the program committee, which met simultaneously in four locations in the US, Europe, and Canada, linked via a video-conference bridge. The video-conferencing facilities were generously provided by AT&T Bell Laboratories, BNR, and Politecnico di Torino, and we thank them all for their support. The globally distributed program committee meeting is one of the indicators of the truly international nature of VTS, which is also reflected in the fact that this year we received paper submissions from authors representing more than 25 countries around the world.

In addition, VTS is introducing a new social program that includes a tour of New York City and a Broadway musical. We hope that this will help the attendees relax and punctuate the technical discussions with a cultural diversion.

The VLSI Test Symposium is the result of a significant amount of volunteer work by many dedicated test professionals including the reviewers, the Program Committee members, the Best Paper Award selection judges, the Advisory Committee, and the Steering Committee. We wholeheartedly thank all of them. We also wish to acknowledge and extend our gratitude to the authors who submitted their work to VTS'96 and to the program participants for agreeing to present their contributions at the symposium. Finally, we would like to thank the IEEE Computer Society, the IEEE Computer Society Test Technology Committee (TTTC), and the IEEE Philadelphia Section for their continued sponsorship and support.

VTS is *your* symposium and we encourage your active participation. We hope that you will find VTS'96 to be beneficial, interesting, thought-provoking, and above all, fun.

Welcome to VTS'96!

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Program Chair

Yervant Zorian
General Chair

Steering Committee

General Chair

Yervant Zorian
AT&T Bell Laboratories
P.O. Box 900
Princeton, NJ 08542
609-639-3176
yz@mach.att.com

Vice General Chair &
Advisory Committee Member

Mukund Modi
Naval Air Warfare Center
Code 4832, Bldg. 551-1
Lakehurst, NJ 08733
908-323-7002
mmodi@aol.com

Program Chair

Rabindra K. Roy
NEC USA
4 Independence Way
Princeton, NJ 08540
609-951-2976
roy@ccrl.nj.nec.com

Finance Chair

Kaushik Roy
Purdue University
Dept. of EE
West Lafayette, IN 47907
317-494-2361
kaushik@ecn.purdue.edu

Program Vice Chair

Michael Nicolaidis
TIMA
46 Ave. Félix Viallet
38031 Grenoble, Cedex, France
+33 76574619
nic@verdon.imag.fr

Program Vice Chair

Adit D. Singh
Auburn University
Dept. of EE
Auburn, AL 36830
334-844-1847
adsingh@eng.auburn.edu

Local Arrangements Chair &
Advisory Committee Member

Wesley E. Radcliffe
IBM, Dept. 798, Bldg. 173
5600 Cottle Road
San Jose, CA 95193
408-282-3051
radcliff@sjmvm16.vnet.ibm.com

Publicity Chair

Sreejit Chakravarty
SUNY Buffalo
Dept. of CS
Buffalo, NY 14260
716-645-3180 ext. 109
sreejit@cs.buffalo.edu

Publication Chair

Andre Ivanov
Univ. of British Columbia
Dept. of EE
Vancouver, BC V6T1Z4 CA
604-822-6936
ivanov@ee.ubc.ca

Tutorials Chair

James A. Monzel
IBM Z/862C
1000 River Street
Essex Jct., VT 05452
802-769-6428
jmonzel@vnet.ibm.com

Audio-Visual Chair

Warren H. Debany
Rome Labs/ERDA
525 Brooks Rd., Bldg. 3
Griffiss AFB, NY 13441-4505
315-330-2922
debanyw@rl.af.mil

Advisory Committee Member

Daniel J. Graham
inTest Corporation
12 Springdale Road
Cherry Hill, NJ 08003
609-424-6886
dgraham170@aol.com

Advisory Committee Member

Ned Kornfield
Widener University
School of Engineering
Chester, PA 19013
215-499-4055
ned613@aol.com

Advisory Committee Member

Prab Varma
CrossCheck Technology
2833 Junction Ave., Ste. 100
San Jose, CA 95134
408-432-9200 ext. 245
prab@crosscheck.com

Support Staff

Judy A. Clark
NEC USA
4 Independence Way
Princeton, NJ 08540
609-951-2443
clark@ccrl.nj.nec.com

Joyce A. Cesario
AT&T Bell Labs
P.O. Box 900
Princeton, NJ 08542
609-639-3196
jac@mach.att.com

JoAnn Groch
NEC USA
4 Independence Way
Princeton, NJ 08540
609-951-2442
groch@ccrl.nj.nec.com

14th IEEE VLSI Test Symposium Program Committee

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IEEE Computer Society
Test Technology Technical Committee

Purpose: TTTC is a volunteer professional organization sponsored by the IEEE Computer Society. The goals of TTTC are to contribute to members' professional development and advancement and to help them solve engineering problems in electronic test.

Membership: TTTC membership is open to all individuals interested in test engineering at a professional level. Members receive Newsletters, announcements, benefits by personal association with other test professionals and opportunities to serve on a wide range of committees. All activities are led by volunteer members.

Dues: There are NO dues for TTTC membership and no parent-organization membership requirements. However, substantial reductions in the fees for TTTC-sponsored meetings and tutorials are available to members of IEEE and/or IEEE Computer Society.

Newsletter: Every year TTTC publishes four issues of its newsletter embedded in the magazine IEEE Design & Test of Computers. In addition TTTC publishes several issues of a more comprehensive newsletter that is mailed to all members. The newsletters cover current issues in test, TTTC technical activities, standards, technical meetings, etc.

Standards: TTTC actively initiates, nurtures and encourages new test standards. Several TTTC-sponsored Working Groups have produced IEEE standards, e.g. the 1149 series, that are used throughout the industry.

Technical Activities: TTTC sponsors a number of Technical Activity Committees (TACs) that address emerging test technology topics. TTTC TACs guide a wide range of activities in these topic areas.

Technical Meetings: TTTC sponsors several well-known conferences and symposia and holds numerous regional and topical workshops which provide opportunities to discuss current test problems and solutions.

Tutorials: TTTC holds tutorials on popular and emerging test topics in conjunction with its larger meetings.

TTTC On-Line: The TTTC Web Site at http://www.computer.org/tab/tttc.html offers samples of the TTTC Newsletter, information about technical activities, conferences, workshops and standards, and links to the Web pages of a number of TTTC-sponsored technical meetings.

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Technical Activities:	Y. Zorian	*AT&T Bell Laboratories, USA*	yz@mach.att.com
Technical Meetings:	W. Radcliffe	*IBM, USA*	radcliff@sjmvm16.vnet.ibm.com
Tutorials:	T. Storey	*Loral, USA*	tstorey@lfs.loral.com
Standards:	Vacant		
Europe:	P. Prinetto	*Politecnico di Torino, Italy*	paolo.prinetto@polito.it
Asia:	K. Kinoshita	*Osaka University, Japan*	kozo@ap.eng.osaka-u.ac.jp

TTTC Sponsored Meetings — 1996

Feb. 6-9	**BAST Workshop**	*Bodega Bay, CA, USA*	E. McCluskey
Mar. 11-14	**European Design & Test Conference**	*Paris, France*	C. Lopez Barrio
Apr. 23-26	**DFT/BIST Workshop**	*Vail, CO, USA*	T. Williams/R. Sedmak
Apr. 26	**Asian Test Workshop**	*Singapore*	W. Moorhead
Apr. 28-May 1	**VLSI Test Symposium**	*Princeton, NJ, USA*	Y. Zorian
May 6-8	**Test Synthesis Workshop**	*Santa Barbara, CA, USA*	T. Cheng
May 15-18	**Mixed-Signal Test Workshop**	*Quebec City, Canada*	B. Kaminska
May 30-31	**North Atlantic Test Workshop**	*Hanover, NH, USA*	J. Karrfalt
Jun. 9-12	**South West Test Workshop**	*San Diego, CA, USA*	W. Mann
Jun. 12-14	**European Test Workshop**	*Sete, France*	C. Landrault
Jun. 19-21	**Rapid Systems Prototype Workshop**	*Thessaloniki, Greece*	N. Kanapoulos
Jul. 8-10	**On-Line Test Workshop**	*Biarritz, France*	M. Nicolaidis
Aug. 13-14	**Memory Test Workshop**	*Singapore*	S. Khim
Sept. 15-18	**MCM Test Workshop**	*Napa, CA, USA*	Y. Zorian
Sept. 24-26	**Hierarchical Test Workshop**	*St. Augustin, Germany*	W. Geisselhardt
Sept. 25-27	**Therminic Workshop**	*Budapest, Hungary*	B. Courtois
Oct. 20-24	**International Test Conference**	*Washington, DC, USA*	C. Hawkins
Oct. 25	**IDDQ Test Workshop**	*Washington, DC, USA*	Y. Malaiya
Nov. 20-22	**Asian Test Symposium**	*Taiwan*	C. Len Lee

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V.S. Sukumaran Nair, *Southern Methodist University*
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Michael Nicolaidis, *TIMA*
Phil Nigh, *IBM Microelectronics*
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P. Pal Chaudhuri, *Indian Institute of Technology, Kharagpur*
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R. A. Parekhji, *IMAG/TIMA*
Sungju Park, *Hanyang University*
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Janak H. Patel, *University of Illinois, Urbana*
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Jeff Rearick, *Hewlett-Packard*
Sudhakar M. Reddy, *University of Iowa*
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Gordon W. Roberts, *McGill University*
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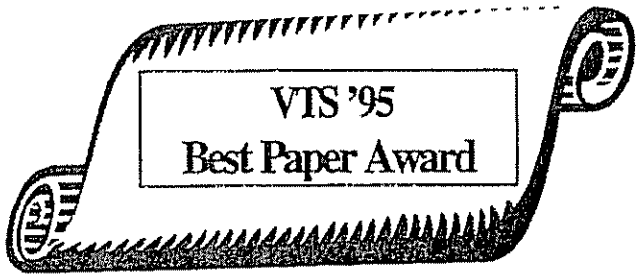

Each year, the VLSI Test Symposium is proud to present the Best Paper Award to the authors of the most outstanding paper. The candidates for this coveted honor are first selected based solely on the numerical ratings of the reviewers and symposium attendees, as recorded on the review forms and the session rating cards. The VTS Best Paper Award Judges then carefully review the candidate papers as published in the proceedings and record the votes.

The paper selected by the VTS '95 Best Paper Award Judges as the most outstanding paper in 1995 is

"Arithmetic Built-In Self Test for High-Level Synthesis"

by N. Mukherjee, M. Kassab, and J. Tyszer of McGill University, and J. Rajski of Mentor Graphics Corporation

In this paper, the authors propose an entirely new built-in self test scheme for high-level synthesis of data path architectures that make use of arithmetic blocks in the data path to generate test vectors and compact test responses.

Congratulations to the winners!

1995 VTS Best Paper Award Judges

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Mel Breuer
University of Southern California

John Hayes
University of Michigan

Nick Kanopoulos
Research Triangle Institute

Prem Menon
University of Massachusetts

Mani Soma
University of Washington

Overview of Tutorials

Tutorial 1

Design Verification and Diagnosis

Dhiraj Pradhan, Texas A&M University
Jacob Abraham, University of Texas at Austin

Description:

This tutorial will cover both fundamentals and advances in design verification. With 100+ million transistor chips becoming a reality, traditional hardware verification methods using simulation have been proven inadequate. Part of the tutorial will discuss a unified approach using Binary Decision Diagram representations of Boolean functions and finite-state machines to formally verify the correctness of hardware designs and implementations from the transistor level up to the behavioral level. It will cover current practice in industry as well as recent research results in these areas, including the use of abstractions and partitioning to improve the problem of state space explosion. Recent developments in verification using ATPG based methods such as Recursive Learning will also be discussed. State-of-the-art university tools in this field will be described, and examples of verifying real chips from industry application of the tools will be included. Open problems and directions for research will also be pointed out. Attendees will receive copies of the notes and key publications.

Tutorial 2

New Trends in Designing and Testing VLSI Systems

Sujit Dey, NEC USA
Peter Marwedel, University of Dortmund

Description:

This tutorial provides a comprehensive overview of the new methodologies that are emerging for the design of electronic systems, including high level synthesis, system level synthesis, hardware-software co-design, and core-based design. Various design and analysis issues of each of the advanced methodologies will be discussed, with special emphasis on the testing challenges and opportunities that arise with each new design methodology. Existing test generation and design-for-testability techniques to generate testable non-scan, partial scan, and BIST designs from RT-level, behavioral, and system level specifications are reviewed. Core-based design will be motivated and its consequences will be analyzed. Consequences that will be discussed, will include, for example, the need for hardware-software co-design environments, requirements for compilers, and opportunities for testing. Attendees will receive copies of the notes.

EXHIBIT E

Proceedings

IEEE

European Test Workshop

Montpellier (Hotel la Corniche in Sète), France

June 12 – 14, 1996

Sponsored by

IEEE Computer Society Technical Committee on Test Technology

Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier

Table of Contents

Foreword

This Compendium of the presentations of the 1st European Test Workshop reflects the high quality and the variety of the research in electronic testing currently done in Europe. The program was selected out of 91 submissions from 21 European, 3 American, and 2 Asian countries. In order to keep space for a lively and interesting discussion only 27 contributions could be presented in regular sessions, and 32 contributions were selected as poster presentations. Due to this high competitiveness you will find many excellent papers also in the poster sessions, and all accepted submissions are included in this compendium if the authors provided an appropriate text. In some cases a clearance for written material was not given, and only an oral presentation was possible.

We hope that the efforts of the entire organizing committee will make ETW an enjoyable and profitable experience. All the members of the microelectronic department at LIRMM have worked hard to make ETW a success. Special thanks go to Yves Bertrand, Christian Dufaza, Marie-Lise Flottes, Patrick Girard, Pascal Nouet, Serge Pravossoudovitch, Michel Renovell and Bruno Rouzeyre for their dedication in the pre-conference preparation.

The announcement of the 1st ETW'96 received an overwhelming response, and hopefully it will be the initial event of a series of exciting and interesting workshops in Europe.

Welcome to the1st IEEE European Test Workshop !

Hans-Joachim Wunderlich

Program co-Chair

Christian Landrault

General Chair

Steering Committee

General Chair: Christian Landrault – LIRMM – F
Vice General Chair: Paolo Prinetto – Politecnico di Torino – I
Program Chairs: Hans J. Wunderlich – University of Siegen – Germany
Kees Baker – Philips – NL
IEEE-CS Liaison: T.W. Williams – IBM – USA
Finance: Serge Pravossoudovitch – LIRMM – F
Local Arrangements: Yves Bertrand – LIRMM – F
Publicity: Michael Nicolaidis – TIMA/INPG – F
Registration: Bruno Rouzeyre – LIRMM – F

Program Committee

E.J. Aas – U of Trondheim – N
Stefano Barbagallo – Italtel – I
R. G. Bennetts – Synopsys – UK
Bernard Courtois – TIMA CMP – F
Joan Figueras – Universidad Politechnica de Catalunya – SP
Hideo Fujiwara – Nara Institute of Science & Technology – J
Christophe Gauthron – Compass Design Automation – F
Susanne Griep – Siemems AG – Germany
Jan Hlavicka – Czech Technical University – Cz
Andrzej Hlawiczka – Silessian Technical University of Gliwice – PL
Hans Kerkhoff – University of Twente – NL
Gerd Krueger – Siemens–Nixdorf AG – Germany
Carlos Lopez–Barrio – Telefonica I + D – SP
David Medina – Italtel SIT – I
Hans Manhaeve – KHBO – B
Piero W. Olivo – Universita di Bologna – I
Antonis Paschalis – National Centre for Scientific Research – GR
Michel Renovell – LIRMM – F
J. Paulo Teixeira – INESC – P
Raimund Ubar – Tallinn Technical University – EE
Ralph Wagner – Robert Bosch GmbH – Germany
Michael Wahl – University of Siegen – Germany
T.W. Williams – IBM – USA
Yervant Zorian – Lucent Bell Lab – USA

EXHIBIT F

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Ex Parte Reexamination Filing Data - March 31, 2005

1. Total requests filed since start of ex parte reexam on 07/01/81 7490

a. By patent owner	3143	42%
b. By other member of public	4182	56%
c By order of Commissioner	165	2%

2. Number of filings by discipline

a. Chemical Operation	2346	31%
b. Electrical Operation	2361	32%
c Mechanical Operation	2783	37%

3 Annual Ex Parte Reexam Filings

Fiscal Yr.	No.	Fiscal Yr.	No.	Fiscal Yr.	No.	Fiscal Yr.	No.
1981	78 (3 mos.)	1989	243	1997	376	2005	256 YTD
1982	187	1990	297	1998	350		
1983	186	1991	307	1999	385		
1984	189	1992	392	2000	318		
1985	230	1993	359	2001	296		
1986	232	1994	379	2002	272		
1987	240	1995	392	2003	392		
1988	268	1996	418	2004	441		

4. Number known to be in litigation 1620 22%

5. Determinations on requests 7240

a. No. granted ..... 6589 ..... 91%

(1) By examiner	6483
(2) By Director (on petition)	106

b. No. denied ..... 651 ..... 9%

(1) By examiner	616
(2) Order vacated	35

6. Total examiner denials (includes denials reversed by Director) 722

a. Patent owner requester	417	58%
b Third party requester	305	42%

7. Overall reexamination pendency (Filing date to certificate issue date)

a. Average pendency	21.6 (mos.)
b. Median pendency	16.9 (mos.)

8. Reexam certificate claim analysis:

	Owner Requester	3rd Party Requester	Comm'r Initiated	Overall
a. All claims confirmed	39%	60%	1%	26%
b. All claims cancelled	31%	64%	5%	10%
c. Claims changes	47%	50%	3%	64%

9 Total ex parte reexamination certificates issued (1981 - present) 5094

a. Certificates with all claims confirmed	1328	26%
b. Certificates with all claims canceled	510	10%
c. Certificates with claims changes	3256	64%

10. Reexam claim analysis - requester is patent owner or 3rd party; or Comm'r initiated

a. Certificates _ PATENT OWNER REQUESTER 2223

(1) All claims confirmed	519	23%
(2) All claims canceled	159	7%
(3) Claim changes	1545	70%

b. Certificates _ 3rd PARTY REQUESTER 2738

(1) All claims confirmed	792	29%
(2) All claims canceled	325	12%
(3) Claim changes	1621	59%

c. Certificates _ COMM'R INITIATED REEXAM 133

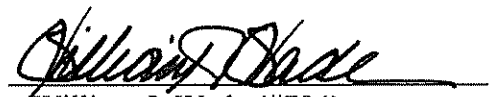
(1) All claims confirmed	17	13%
(2) All claims canceled	26	20%
(3) Claim changes	90	67%

CERTIFICATE OF SERVICE

I HEREBY CERTIFY that on February 6, 2006, I electronically filed the foregoing document with the Clerk of Court using CM/ECF which will send notification of such filing, and which has also been served as noted:

BY HAND

Karen Jacobs Louden, Esquire
Morris, Nichols, Arsht & Tunnell
1201 North Market Street
Wilmington, DE 19899



William J. Wade (#704)

DATED: February 6, 2006